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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,492	03/18/2004	Raffaele Zambrano	854063.679D1	7636

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EXAMINER	
NGUYEN, HA T	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,492	ZAMBRANO ET AL.	
	Examiner	Art Unit	
	Ha T. Nguyen	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 18 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3-18-4, [illegible].
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 5, 11-12, 15, and 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Layadi et al. (USPN 6,436,829, hereinafter "Layadi").

Referring to Figs. 2-5 and related text, Layadi discloses [Re claim 1] a process for manufacturing an integrated device, comprising the steps of: forming a first conductive region 220, 530; forming an insulating layer 201, 580 which coats said first conductive region; forming a through opening in said insulating layer above said first conductive region; forming a contact structure 214, 215, 230 in said through opening, said contact structure comprising a conductive material layer 214, 215, 230 delimiting a region 333; and forming a second conductive region 560 above said through opening of said insulating layer; wherein said region delimited by said contact structure is left empty.

[Re claim 11] Layadi discloses a process for manufacturing an integrated device, comprising forming a first conductive region; forming an insulating layer on the first conductive region; forming a through opening in the insulating layer above the first conductive region; forming a conductive material layer on walls of the through opening, the conductive material layer contacting the first conductive region and surrounding an empty region; and forming a second conductive region over the empty region, as shown above, it also discloses the second conductive region closing the through opening and empty region (see Figs. 4-5).

[Re claim 21] Layadi discloses a process of making an integrated device, comprising; forming a first conductive region; forming an insulating layer on the first conductive region; forming a through opening extending in the insulating layer; forming a contact structure in the through opening, the contact structure comprising a conductive material layer and an empty region, the conductive material layer being electrically connected to the first conductive region; and forming a cover layer above the contact structure and covering the empty region, as shown above;

[Re claims 2 and 12] wherein said conductive material layer is obtained by depositing a titanium layer 214;

[Re claims 5 and 15] wherein said conductive material layer is obtained by depositing a titanium- nitride layer 215;

[Re claims 22 and 23] wherein the covering layer is a conductive layer that contacts the conductive material layer of the contact structure; and wherein the conductive material has a side surface and a bottom surface that faces the first conductive region, and the empty region is surrounded by the conductive material layer (see Fig. 5).

Claim Rejections - 35 USC. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was

made in order for the examiner to consider the applicability of 35 U.S.C. 103□ and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-8 and 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan (USPN 6376369) in view of Ohba (USPN 6355545).

Referring to Figs. 6-10 and related text, Doan discloses [Re claim 1] a process for manufacturing an integrated device, comprising the steps of: forming a through opening in a substrate 110; forming a contact structure 114, 116 in said through opening, said contact structure comprising a conductive material layer 114, 116 delimiting a region 112; and forming a second conductive region 118 above said through opening; wherein said region delimited by said contact structure is left empty. But it fails to disclose expressly forming a first conductive region; forming an insulating layer which coats said first conductive region. However, the missing limitations are well known in the art because Ohba discloses these features (See Fig. 7, Wiring B and dielectrics). A person of ordinary skill is motivated to modify Doan with Ohba to obtain multi-level interconnects.

[Re claim 21] The combined teaching of Doan and Ohba discloses a process of making an integrated device, comprising; forming a first conductive region; forming an insulating layer on the first conductive region; forming a through opening extending in the insulating layer; forming a contact structure in the through opening, the contact structure comprising a conductive material layer and an empty region, the conductive material layer being electrically connected to the first conductive region; and forming a cover layer above the contact structure and covering the empty region, as shown above.

[Re claim 2] Doan also discloses wherein said conductive material layer is obtained by depositing a titanium layer 215;

[Re claim 5] wherein said conductive material layer is obtained by depositing a titanium-nitride layer 214.

[Re claims 4, 7-8, 27] The combined teaching of Doan and Ohba does not disclose expressly wherein said step of forming said second conductive region comprises depositing conductive material in a non-conformal way over said region, the thicknesses of the Ti and TiN layers and the dimensions of the opening. However, it would have been obvious for an ordinary

artisan to use sputtering to deposit the second conductive region to avoid contamination associated with CVD and to use an appropriate thickness to form an adhesion and a barrier layer. Besides, the examiner takes Official Notice that the claimed width of the opening is commonly used in semiconductor to obtain devices of small size.

Doan also discloses [Re claim 3] wherein said titanium layer is deposited by PVD; [Re claim 6] wherein said titanium-nitride layer is deposited by CVD; [Re claim 26] wherein forming the conductive material layer includes depositing a first conductive layer by PVD and depositing a second conductive layer by CVD; [Re claim 28] wherein the first conductive layer includes titanium and the second conductive layer includes titanium nitride (see col. 7, lines 24-46);

[Re claims 22 and 23] Doan also discloses wherein the covering layer is a conductive layer that contacts the conductive material layer of the contact structure; and wherein the conductive material has a side surface and a bottom surface that faces the first conductive region, and the empty region is surrounded by the conductive material layer; [Re claim 24] wherein the conductive material layer is formed by steps including: coating a side surface of the insulating layer, which laterally defines the through opening, with a coating portion; and forming a horizontal portion that extends on top of the insulating layer and beneath the covering layer(see Fig. 6).

[Re claim 25] The combined teaching of Doan and Ohba discloses substantially the limitations of claim 25, as shown above. But it does not disclose expressly the titanium nitride layer laterally defining the empty region. However, the examiner takes Official Notice that W and TiN are equivalently used as barrier and interconnect materials. It would have been obvious to use TiN instead of W to reduce material requirements.

Therefore, it would have been obvious to combine Doan with Ohba to obtain the invention as specified in claims 1-8 and 21-28 .

5. Claims 13-14 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Layadi , as applied above, in view of Doan.

Layadi discloses substantially the limitations of claims 13-14 and 16-19, as shown above.

But it fails to disclose expressly the details about the method of depositing Ti and TiN and their thicknesses and the opening width.

However, the missing limitations are well known in the art because Doan discloses or made obvious these features, as shown above.

A person of ordinary skill is motivated to modify Layadi with Doan to obtain reliable device.

Therefore, it would have been obvious to combine Layadi with Doan to obtain the invention as specified in claims 13-14 and 16-19 .

6. Claims 9-10, 20, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (EP 0793274 A1, hereinafter "Jones") in view of Doan and Ohba, or Layadi and Doan, or Layadi.

Referring to Figs. 3-8 and related text, Jones discloses a process for manufacturing a ferro-electric memory comprising a transistor 51, 52, 56, 57 and a ferro-electric capacitor 92; forming a first conduction region 56 of said transistor in a substrate of semiconductor material; depositing an insulating material 61 on top of said substrate; forming a through opening in said insulating layer above said first conductive region; forming a contact structure in said through opening; forming a covering layer including a ferro-electric material region 922; forming a second conductive region comprising the first plate 921 between said covering layer and the contact structure, the ferro-electric material region 922 being deposited on top of said first plate, and forming a second plate 923 on top of said ferro-electric material region.

But it fails to disclose expressly the details about the contact structure.

However, the missing limitations are well known in the art because Doan and Ohba, or Layadi and Doan, or Layadi discloses these features, as shown above. In the combined teaching of Jones, Doan and Ohba the second conductive region comprises Pt (see Jones # 921 or 923).

A person of ordinary skill is motivated to modify Jones with Doan and Ohba, or Layadi and Doan, or Layadi to obtain a reliable contact structure.

Therefore, it would have been obvious to combine Jones with Doan and Ohba, or Layadi and Doan, or Layadi to obtain the invention as specified in claims 9-10, 20, and 29.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ha T. Nguyen whose telephone number is (571) 272-1678. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM, except the first Friday of each bi-week. The telephone number for Wednesday is (703) 560-0528.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ha Nguyen
Primary Examiner
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